CLAIMS:

1. An integrated circuit (10), preferably a field programmable gate array - FPGA - or an application specific integrated circuit – ASIC -, the integrated circuit (10) comprising:

a level comparator (30) adapted for comparing a level of a comparator input signal and correspondingly providing a comparator output signal (COS),

a sampling unit (40) coupled to the level comparator (30) and being adapted for sampling (SAM) the comparator output signal (COS), and

a bit error test unit (60) adapted to receive the sampled comparator output signal (SAM) and to determine therefrom an indication of a bit error in a sequence of the sampled comparator output signal (SAM).

2. The integrated circuit (10) according to claim 1 or any one of the above claims, further comprising:

a phase shifting unit (70) being adapted to receive and phase-shift a clock signal (CLK) and to provide to the sampling unit (40) a phase-shifted clock signal (CLKP) for controlling a sampling point of the sampling unit (40).

3. The integrated circuit (10) according to the above claim, further comprising:

a control unit (65) being adapted to control (CTR) at least one of the following:

- the phase-shifting of the phase shifting unit (70),
- the comparison level of the level comparator (30),

- operation of the bit error test unit (60).

4. The integrated circuit (10) according to the above claim, wherein the control unit (65) is adapted to be controlled by at least one of the following:

the bit error test unit (60),

an interface unit (90) adapted to be coupled to a unit (100) external with respect to the integrated circuit (10).

5. The integrated circuit (10) according to claim 1 or any one of the above claims, further comprising at least one of:

an input unit (20) adapted to receive an input signal from external with respect of the integrated circuit (10), wherein the input unit (20) comprises:

the level comparator (30) adapted to receiving as the comparator input signal the input signal, or a signal derived therefrom, and

the sampling unit (40);

a processing unit (50) adapted to receive and process the sampled comparator output signal (SAM); and

an output unit adapted to receive a data signal (OUT) from the processing unit (50), to derive therefrom an output signal, and to provide the output signal to external with respect of the integrated circuit (10).

6. The integrated circuit (10) according to claim 1 or any one of the above claims, wherein the level comparator (30) is adapted to provide at least one of the following:

comparing the comparator input signal against a threshold value

representing the comparison level,

comparing a normal signal of the comparator input signal against a complementary signal of the comparator input signal, with the complementary signal being complementary to the normal signal.

7. The integrated circuit (10) according to claim 1 or any one of the above claims, wherein the bit error test unit (60) is adapted to provide at least one of the following:

determining as the bit error indication at least one of the following: the number of bits in the sequence, the number of errors detected in the sequence, the number of error-free bits in the sequence, a value of a bit error rate representing the ratio of detected bit errors per number of bits,

determining the bit error indication by comparing the sampled comparator output signal (SAM) against an expected comparator output signal (COS) preferably representing the comparator output signal (COS) without error,

determining the bit error indication with respect to at least one of the sampling point, preferably representing a point in time relative to transition time of the clock signal (CLK), and the comparison level of the level comparator (30),

storing and/or buffering (80) the bit error indication,

communicating the bit error indication to at least one of: another unit of the integrated circuit, a unit external with respect to the integrated circuit.

8. The integrated circuit (10) according to claim 1 or any one of the above claims, further comprising an interface unit (90), preferably a Joint Test Action Group – JTAG - or Boundary Scan Interface, adapted to be coupled to an external bit error test processing unit (100) being external with respect to the integrated circuit (10), the interface unit (90) being

adapted to provide at least one of the following:

communicating at least one of status information of the bit error test unit (60) and the bit error indication to the external bit error test processing unit (100),

receiving a control signal from the external bit error test processing unit (100) in order to provide at least one of: controlling operation of the bit error test unit (60), initiating operation of the bit error test unit (60), controlling operation of the control unit (65).

9. The integrated circuit (10) according to claim 1 or any one of the above claims, comprising at least one of the features:

the sampling unit (40) comprises a deserializer adapted for deserializing the comparator output signal (COS),

the integrated circuit (10) further comprises a clock data recovery unit (200) adapted to derive the clock signal (CLK) from a data signal, preferably from one of: the comparator input signal, the input signal, a signal derived from the input signal, or the comparator output signal (COS), wherein the phase shifting unit (70) is coupled to the clock data recovery unit and receives the recovered clock signal (CLK) therefrom.

10. A method in an integrated circuit (10), preferably a field programmable gate array - FPGA - or an application specific integrated circuit – ASIC -, the method comprising the steps of:

a) comparing a level of a comparator input signal and correspondingly providing a comparator output signal (COS),

b) sampling (SAM) the comparator output signal (COS),

c) determining from the sampled comparator output signal (SAM) an

indication of a bit error in a sequence of the sampled comparator output signal (SAM).

11. The method of the above claim, further comprising the step of:

d) phase-shifting (CLKP) a clock signal (CLK) for controlling a sampling point of step b).

12. A software program or product, preferably stored on a data carrier, for executing the method of the above claims when run on a data processing system such as a computer.